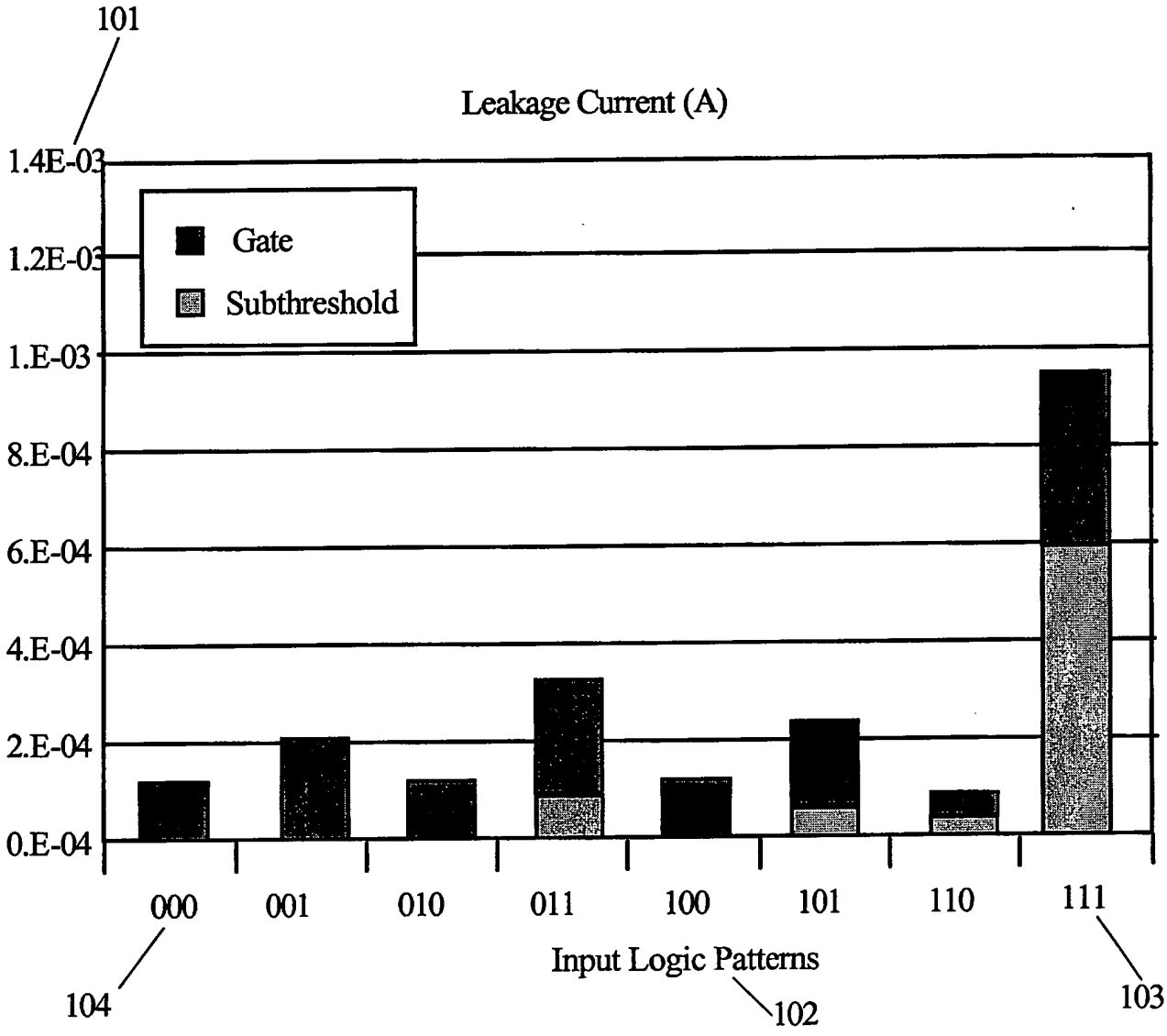
101
Leakage Current (A)
1.4E-03
1.2E-03
1.E-03
8.E-04
6.E-04
4.E-04
2.E-04
0.E-04
Gate
Subthreshold
000
001
010
011
100
101
110
111
Input Logic Patterns
104
102
103

FIG. 1

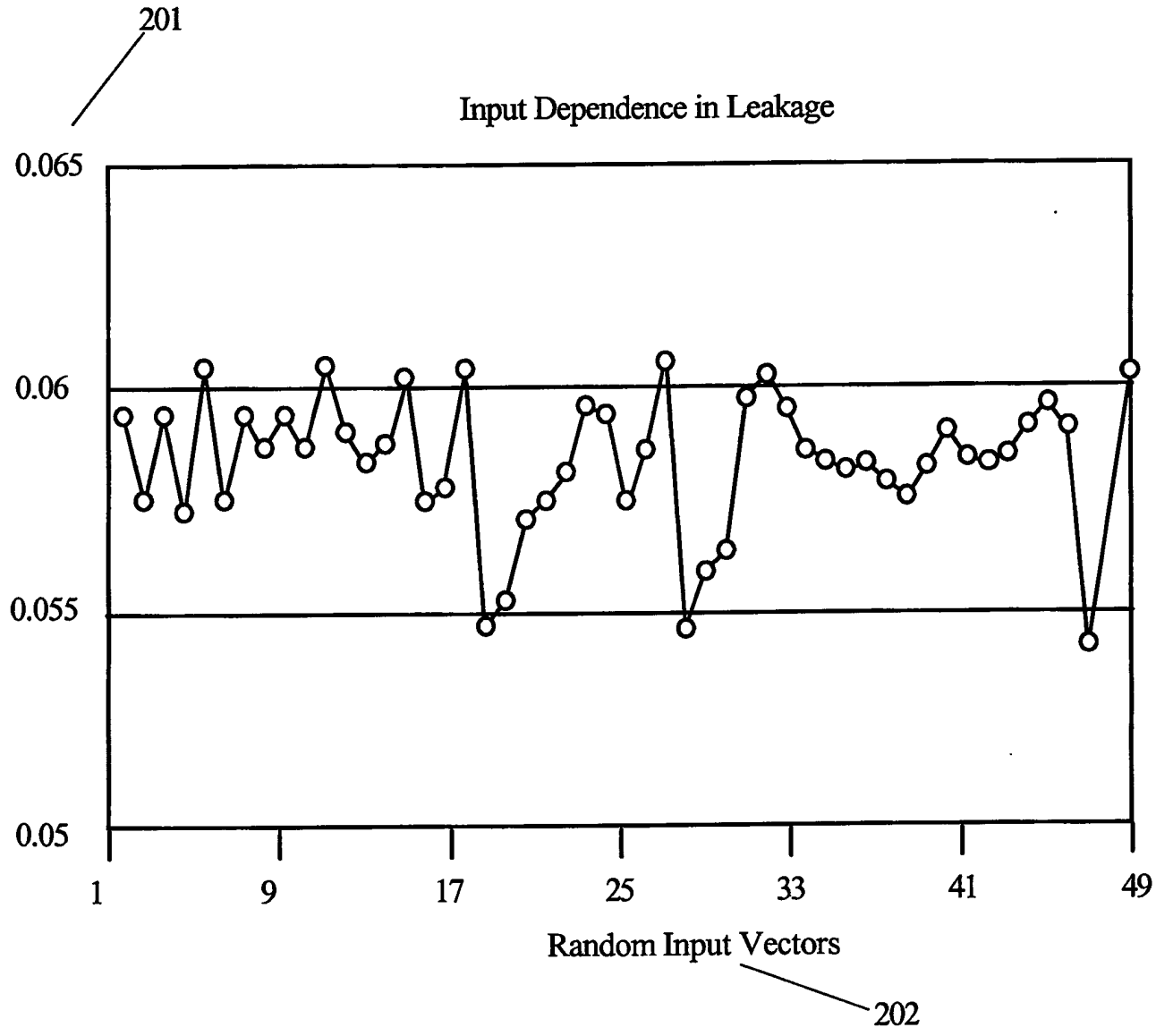
201
Input Dependence in Leakage
0.065
0.06
0.055
0.05
1
9
17
25
33
41
49
Random Input Vectors
202

FIG. 2

301 Circuit	302 # Cells	303 # inputs	304 I_{max}(mA)	305 I_{min}(mA	306 cv.
c432	187	36	0.073899	0.0597	0.0237
c499	222	41	0.21463	0.153863	0.0337
c880	383	60	0.132035	0.095789	0.0335
c1355	566	41	0.173451	0.127854	0.0301
c1908	996	33	0.312824	0.210898	0.0610
c2670	11255	233	0.427436	0.325011	0.0363
c5311	2485	178	0.824406	0.670118	0.0279
c7752	3692	270	0.713998	0.665011	0.0483

FIG. 3

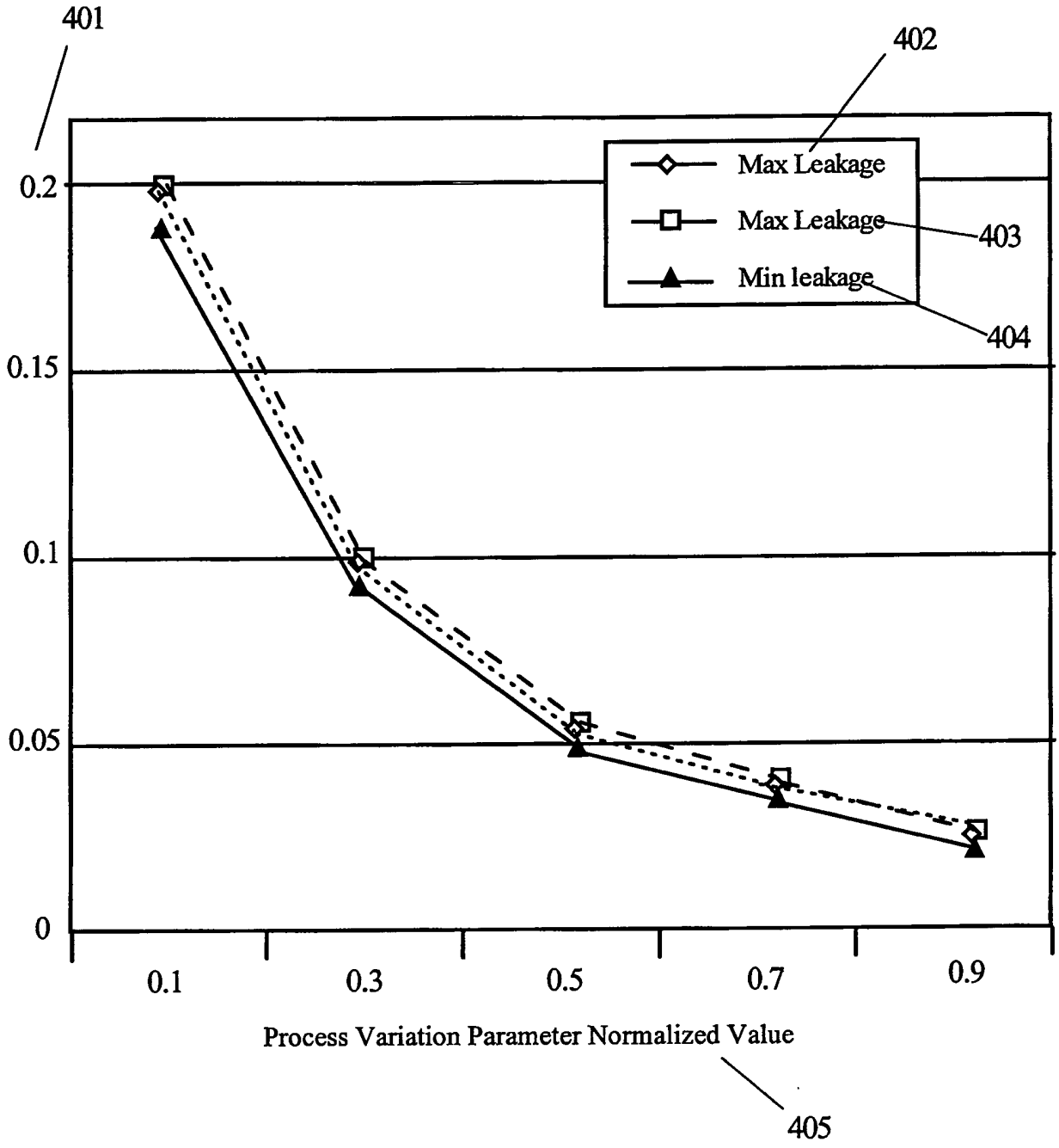
401
402
Max Leakage
Max Leakage
403
Min leakage
404
0.2
0.15
0.1
0.05
0
0.1
0.3
0.5
0.7
0.9
Process Variation Parameter Normalized Value
405

FIG. 4

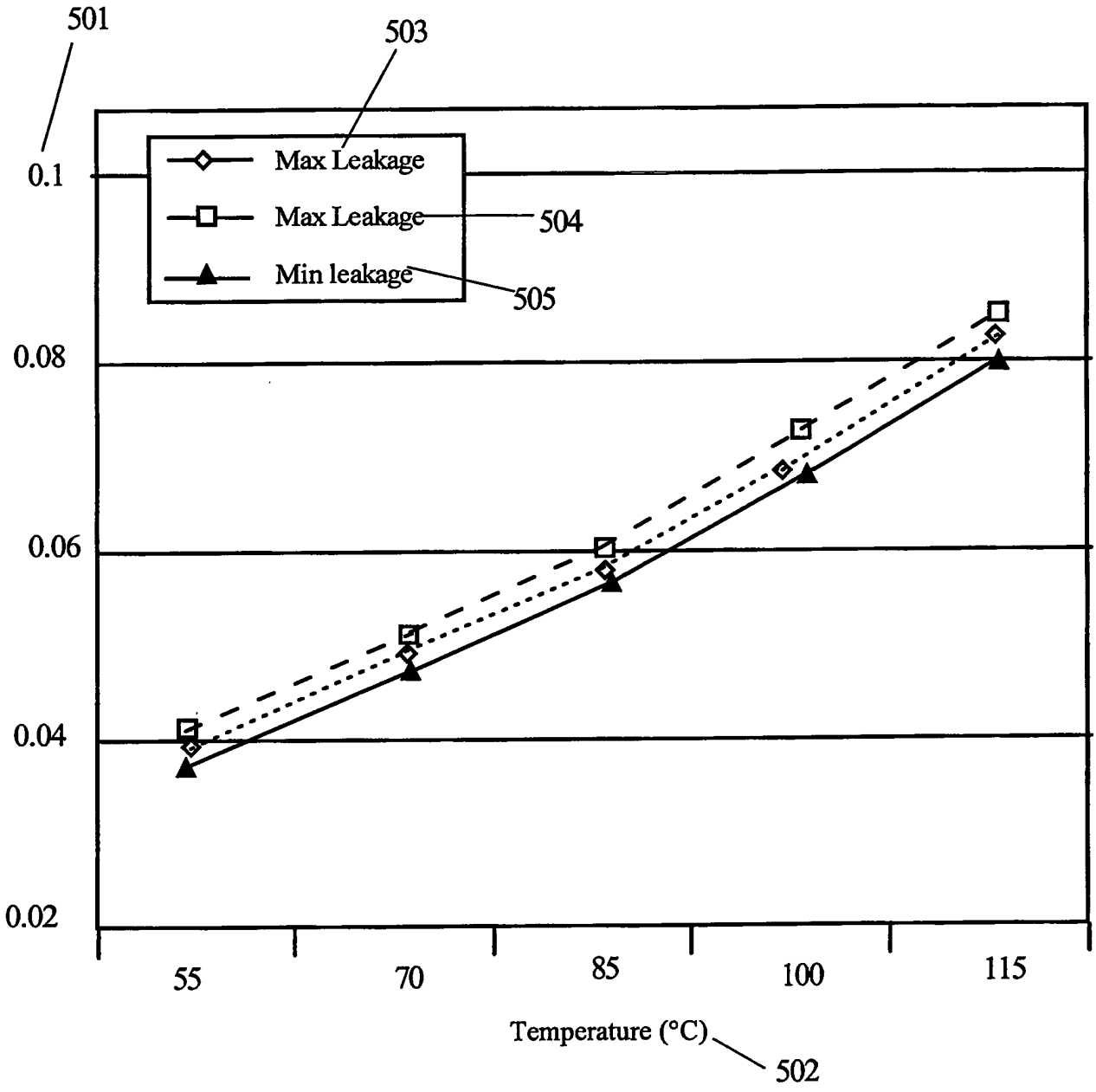
501
503
Max Leakage
Max Leakage
504
Min leakage
505
0.1
0.08
0.06
0.04
0.02
55
70
85
100
115
Temperature (°C)
502

FIG. 5

603 604 605 606 607

State	Gate leakage	Subthreshold Leakage	Total Leakage	State Occurrence Probability
00	G_{00}	S_{00}	$L_{00}=G_{00}+S_{00}$	$(1-P_1)(1-P_2)$
01	G_{01}	S_{01}	$L_{01}=G_{01}+S_{01}$	$(1-P_1)P_2$
10	G_{10}	S_{10}	$L_{10}=G_{10}+S_{10}$	$P_1(1-P_2)$
11	G_{11}	S_{11}	$L_{11}=G_{11}+S_{11}$	P_1P_2

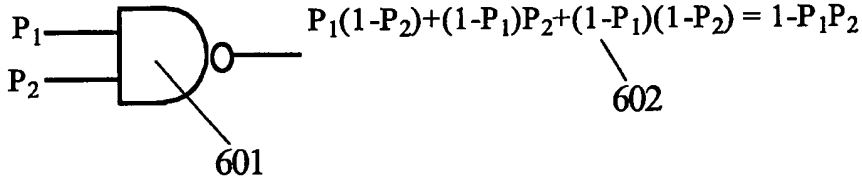

FIG. 6

701 702 703 704

Circuit	Ave Leakage(W)	SP Method (W)	Rel. Error(%)
c432	0.06599	0.06800	3.056
c499	0.17885	0.17786	-0.556
c880	0.10857	0.10927	0.643
c1355	0.13828	0.14236	2.950
c1908	0.22508	0.21437	-4.758
c2670	0.34197	0.34638	1.290
c5311	0.70782	0.71171	0.549
c7752	0.99772	0.97618	-2.158

FIG. 7

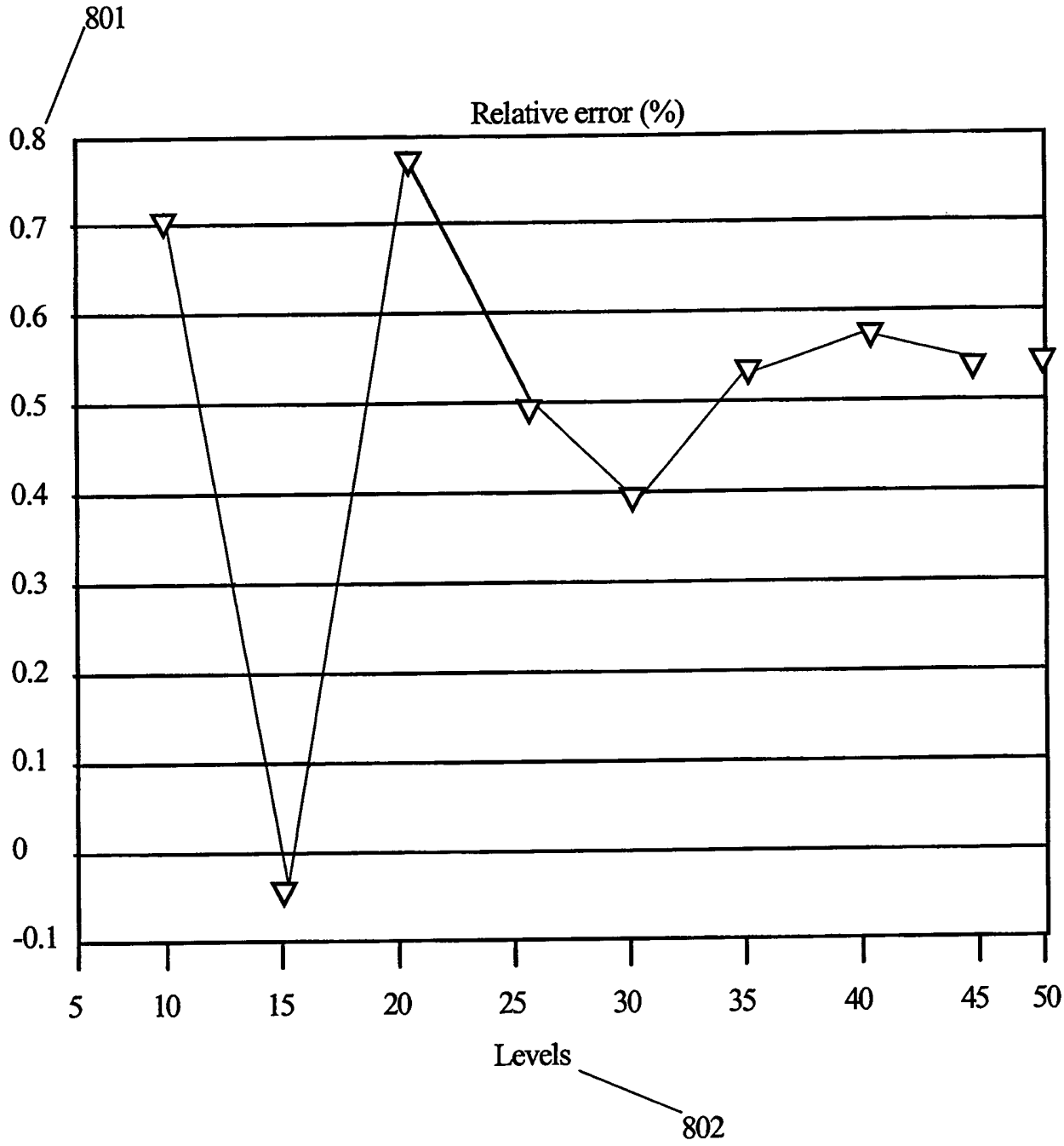
801
Relative error (%)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
5
10
15
20
25
30
35
40
45
50
Levels
802

FIG. 8

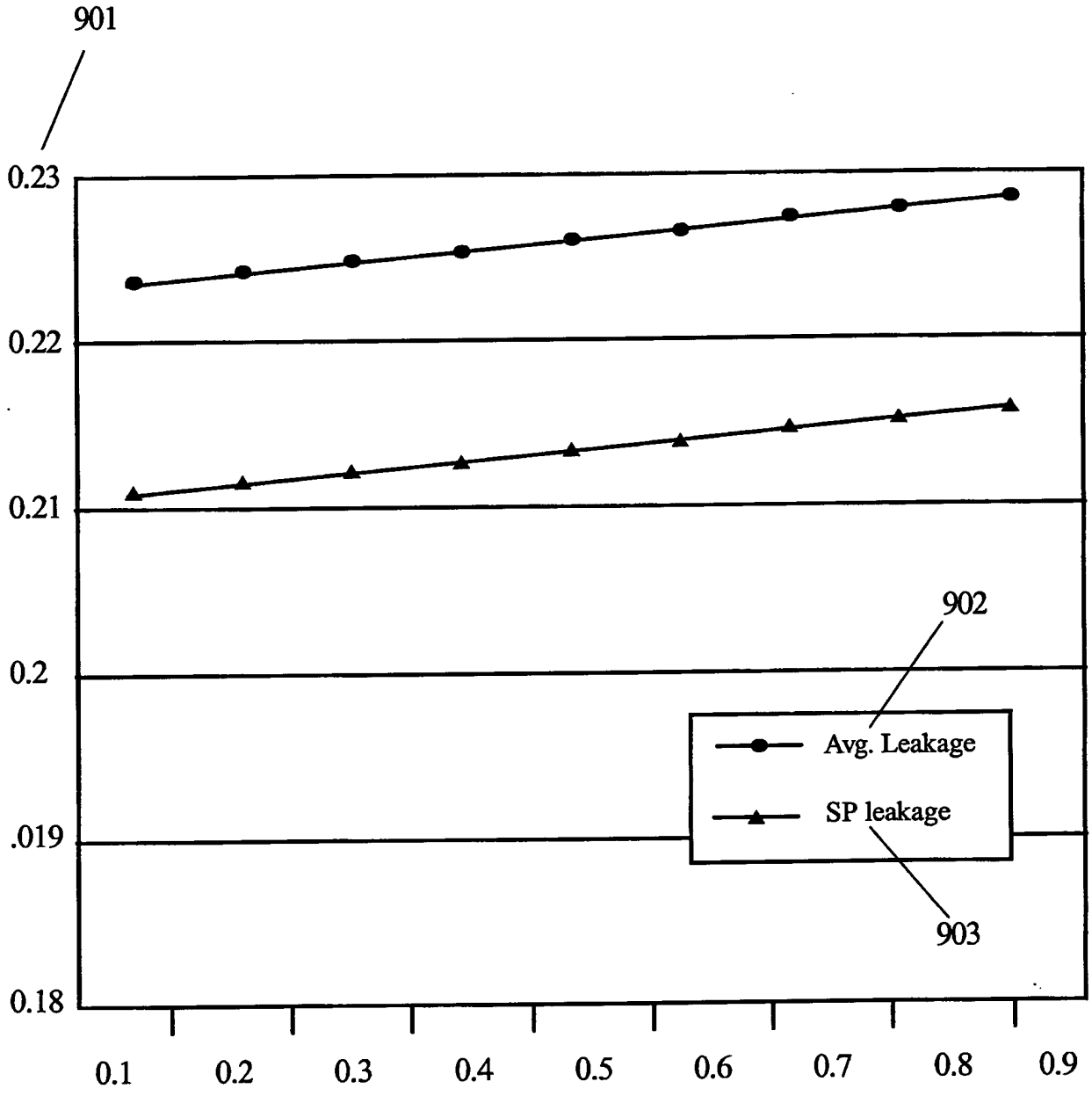
901
0.23
0.22
0.21
0.2
.019
0.18
902
Avg. Leakage
SP leakage
903
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
assigned probability for the first four inputs

FIG. 9

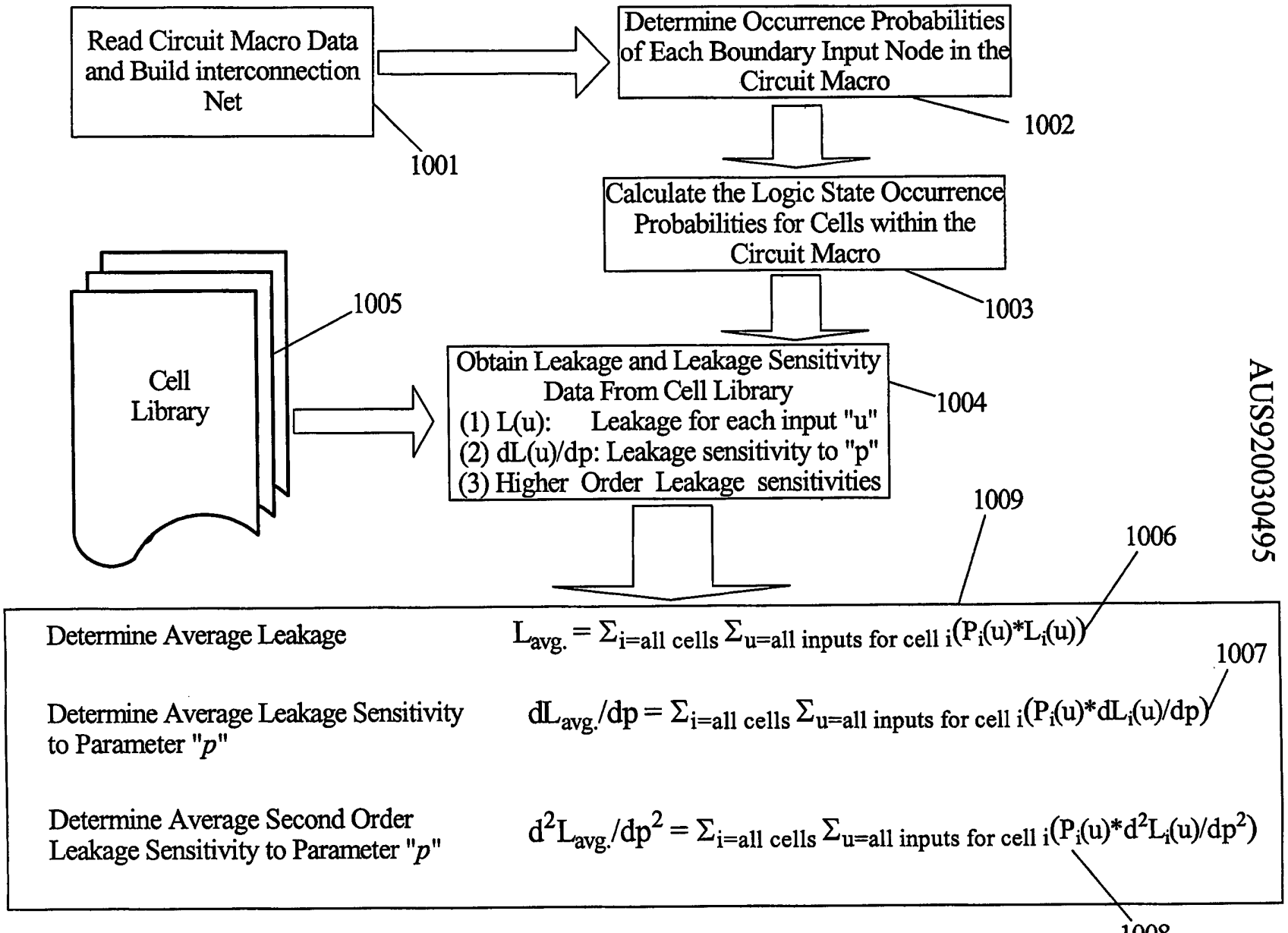
Read Circuit Macro Data and Build interconnection Net
1001
Determine Occurrence Probabilities of Each Boundary Input Node in the Circuit Macro
1002
Calculate the Logic State Occurrence Probabilities for Cells within the Circuit Macro
1003
Cell Library
1005
Obtain Leakage and Leakage Sensitivity Data From Cell Library
(1) L(u): Leakage for each input "u"
(2) dL(u)/dp: Leakage sensitivity to "p"
(3) Higher Order Leakage sensitivities
1004
1009
1006
Determine Average Leakage
$L_{avg.} = \Sigma_{i=all\ cells} \Sigma_{u=all\ inputs\ for\ cell\ i}(P_i(u)*L_i(u))$
1007
Determine Average Leakage Sensitivity to Parameter "p"
$dL_{avg.}/dp = \Sigma_{i=all\ cells} \Sigma_{u=all\ inputs\ for\ cell\ i}(P_i(u)*dL_i(u)/dp)$
Determine Average Second Order Leakage Sensitivity to Parameter "p"
$d^2L_{avg.}/dp^2 = \Sigma_{i=all\ cells} \Sigma_{u=all\ inputs\ for\ cell\ i}(P_i(u)*d^2L_i(u)/dp^2)$
1008

FIG. 10

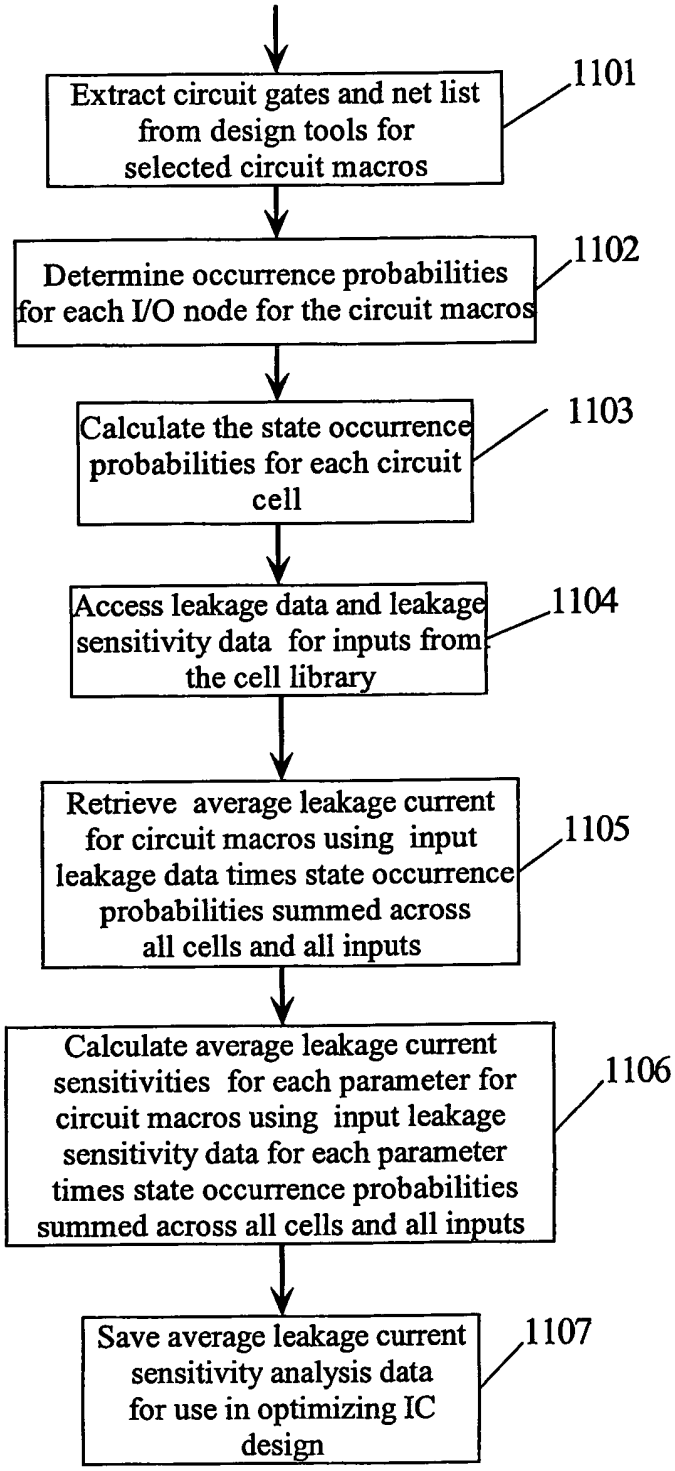
Extract circuit gates and net list from design tools for selected circuit macros
1101
Determine occurrence probabilities for each I/O node for the circuit macros
1102
Calculate the state occurrence probabilities for each circuit cell
1103
Access leakage data and leakage sensitivity data for inputs from the cell library
1104
Retrieve average leakage current for circuit macros using input leakage data times state occurrence probabilities summed across all cells and all inputs
1105
Calculate average leakage current sensitivities for each parameter for circuit macros using input leakage sensitivity data for each parameter times state occurrence probabilities summed across all cells and all inputs
1106
Save average leakage current sensitivity analysis data for use in optimizing IC design
1107

FIG. 11

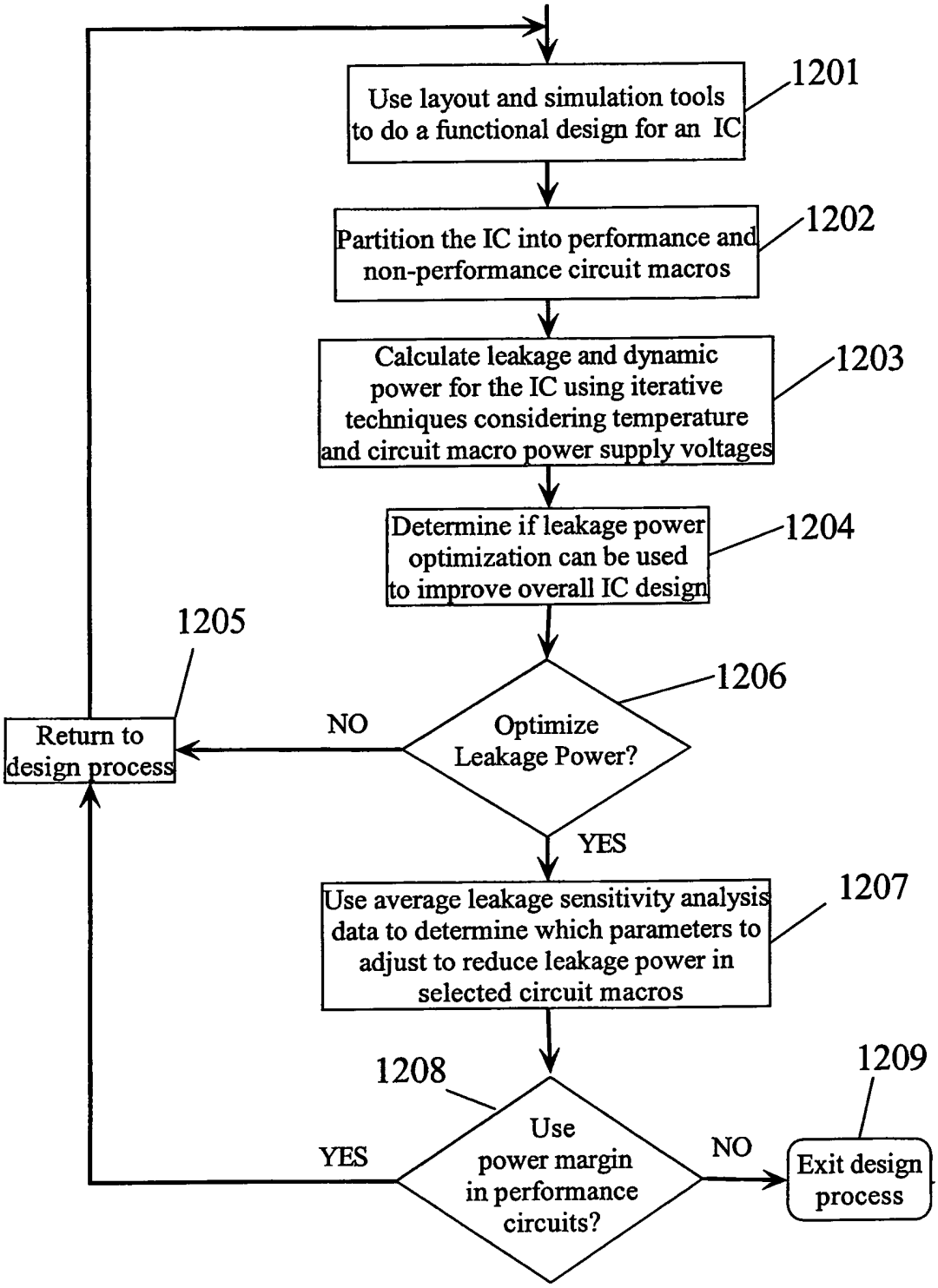
Use layout and simulation tools to do a functional design for an IC
1201
Partition the IC into performance and non-performance circuit macros
1202
Calculate leakage and dynamic power for the IC using iterative techniques considering temperature and circuit macro power supply voltages
1203
Determine if leakage power optimization can be used to improve overall IC design
1204
1205
1206
Optimize Leakage Power?
NO
Return to design process
YES
Use average leakage sensitivity analysis data to determine which parameters to adjust to reduce leakage power in selected circuit macros
1207
1208
1209
Use power margin in performance circuits?
YES
NO
Exit design process

FIG. 12

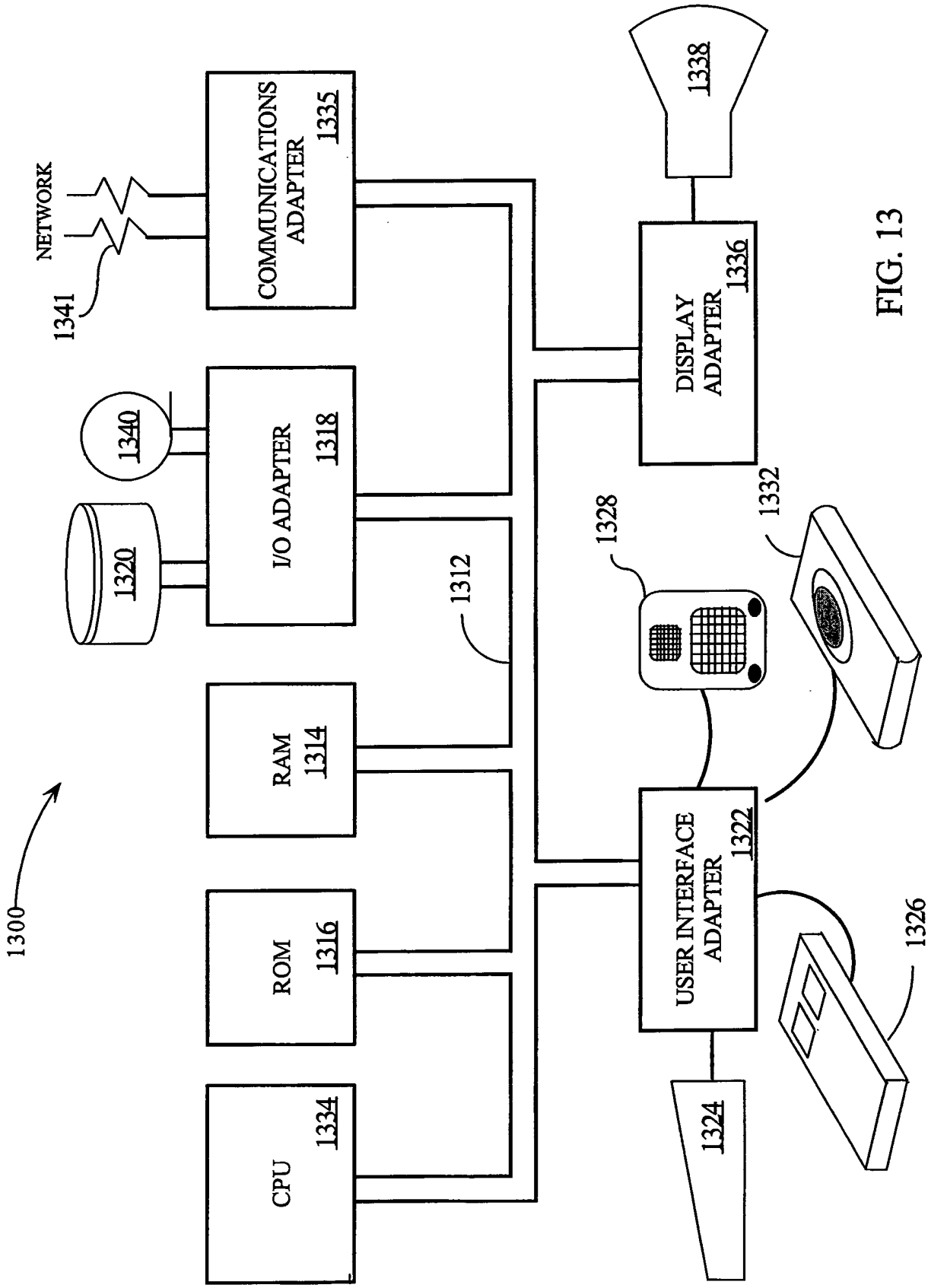
1300
CPU 1334
ROM 1316
RAM 1314
1312
I/O ADAPTER 1318
1320
1340
NETWORK
1341
COMMUNICATIONS ADAPTER 1335
1338
DISPLAY ADAPTER 1336
1328
1332
USER INTERFACE ADAPTER 1322
1324
1326

FIG. 13